94-9SL2-LAFIL-R2

PROCESSING, FABRICATION, AND DEMONSTRATION OF HTS INTEGRATED MICROWAVE CIRCUITS

S. H. Talisa and J. Talvacchio

Cryoelectronics

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Navy Contract No. N00014-91-C-0112
R&D Status Reports # Data Item A0001, Report No. 13
Reporting Period: July 25, 1994 through October 24, 1994

Prepared for

Office of Naval Research
800 N. Quincy Street
Arlington, VA 22217-5000
Project Manager, Dr. W. A. Smith

Westinghouse STC
1310 Beulah Road
Pittsburgh, Pennsylvania 15235-5098

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R&D STATUS REPORT

ARPA Oder No.: 7932 Program Code No.: htsc 051-101

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Effective Date of Contract: 7/24/91

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Principal Investigator: G. R. Wagner

Telephone No.: (412) 256-1436

Short Title of Work: Processing, Fabrication, and Demonstration of HTS Integrated Microwave Circuits

Reporting Period: 7/25/94 to 10/24/94

DESCRIPTION OF PROGRESS

TASK 1.0: COMPARATIVE TECHNOLOGY ASSESSMENT

This task is essentially complete, but we are continuing to monitor progress in other technologies as they relate to the goals of this program.

TASK 2.1: INTEGRATED SUBSYSTEM SPECIFICATIONS

No work on this task was performed during this reporting period.

TASK 2.2: FUNCTIONAL COMPONENT AND SUBSYSTEM DESIGN, FABRICATION AND TESTING

Filterbanks

Universal Test Fixture Fabrication and Testing

A fixture for the testing of microstrip and coplanar circuits has been designed and fabricated. It was made to serve as a universal fixture for all or most of our testing following the substrate size and port location established by the work performed to date on filterbanks. Figure 1 is a photograph of the device showing the connectors and the lid. SMA connectors were used. A second version of this device was also fabricated for tests with the lumped element structures which are in coplanar waveguide configuration (see Lumped Element section below). This second fixture will be used at the Westinghouse Electronics Systems Group, in order to provide a quick turn-around of measurements relevant to the lumped-element design effort.

7-Pole EW Filters

Measurements on the 7-pole single filters (Channel 3 design) fabricated continued during this reporting period. The filters were tested under various packaging conditions, both in the universal test fixture discussed above and in our standard packages. Two identical filters, parallel to each other, were defined on a substrate area the size of one of the filterbank channels (4.74 cm by 2.8 cm) made to date. The substrate and package sizes as well as the connector locations have became standard for

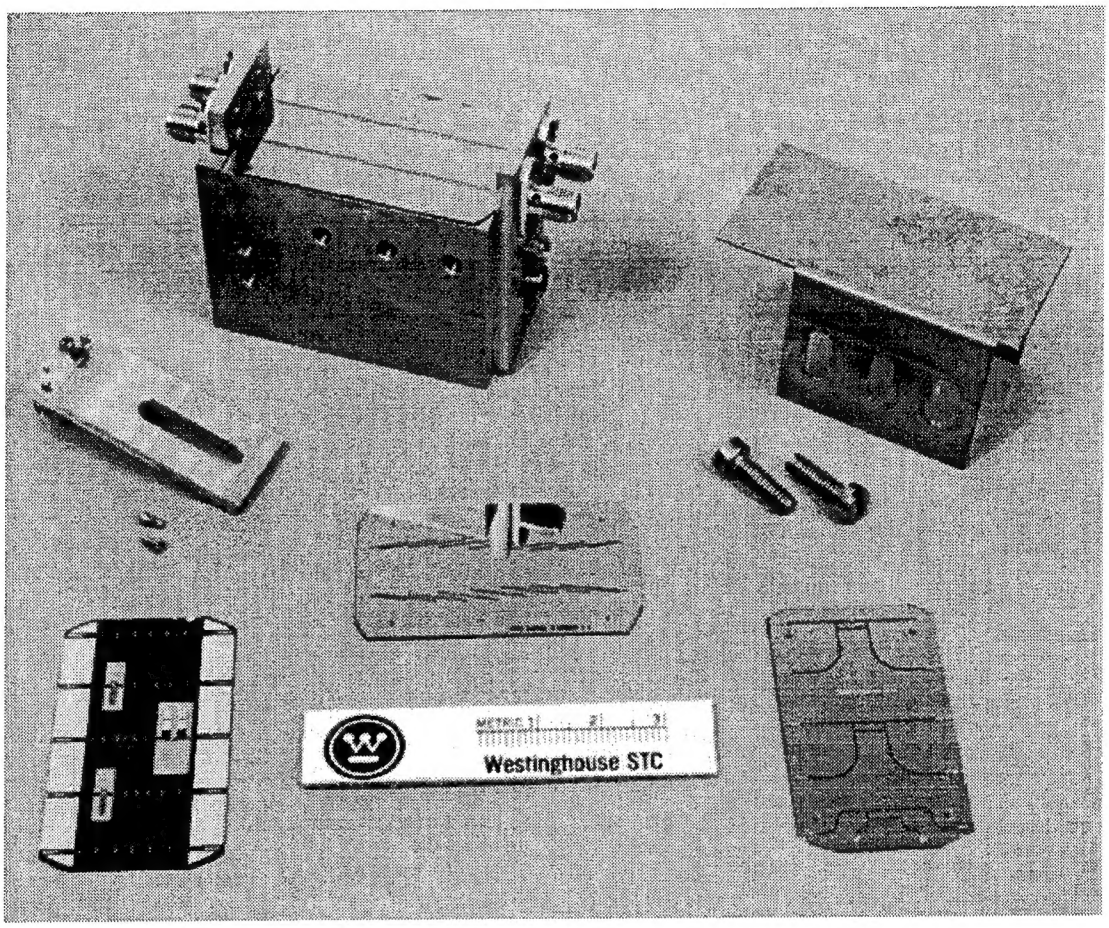


Figure 1 - Photograph of the universal test fixture made showing some of the wafers tested during this reporting period.

this work and we tailor our device layouts and testing to fit this design. Two wafer samples were made; one of them can be seen in the center of Figure 1.

The results were obtained under the various packaging conditions were fairly consistent, although small variations in center frequency and passband shape were observed. Figure 2 are the filter response and both return losses. Two concerns are being investigated: The center frequency deviation from design target (50 to 75 MHz below design goal) and the spurious interfering mode which appears on the lower filter skirt. The latter phenomenon appears to have been predicted by the Sonnet simulation performed on the filter designed, although it is shifted farther away from the center frequency, to a level of about -90 dB. The effects of package and substrate size on this spurious effect will be investigated in the next reporting period.

50Ω Line Tests

Straight 50 Ω microstrip lines were fabricated also on the standard substrate size (shown in Figure 1, mounted on the universal test fixture). These were used to evaluate and help improve the quality of the coaxial-to-microstrip transitions in our packages at the filterbank frequencies of interest. The test lines are also being used to evaluate the quality of our network analyzer calibration so that more precise measurements can be made. This is an ongoing process which is synergistic with our package and connector interface designs. Figure 3 shows insertion and return losses obtained to date.

Tandem Coupler with Gold Wire Crossovers

Fabrication of two wafers with three test tandem couplers each were completed during this reporting period. Figure 4 shows a photograph of one of the wafers. Results for one of the couplers are given in Figure 5. Further testing will continue in the next quarter.

Lumped Elements

Lumped element test structures were designed and fabricated on two sample wafers in this quarter. These are parallel L-C circuits in series with 50-Ω input and output coplanar waveguide lines. Two kinds of resonant L-C circuits were made with the same

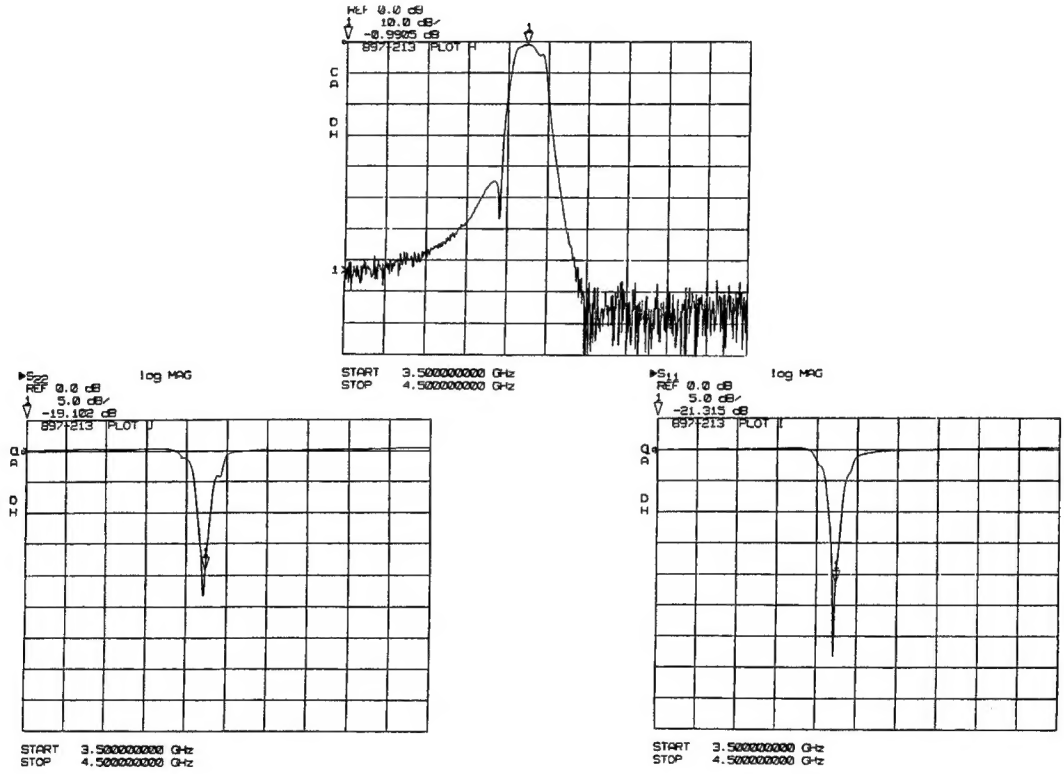


Figure 2 - 7-pole filter results to date. Shown are the insertion loss and the two return losses.

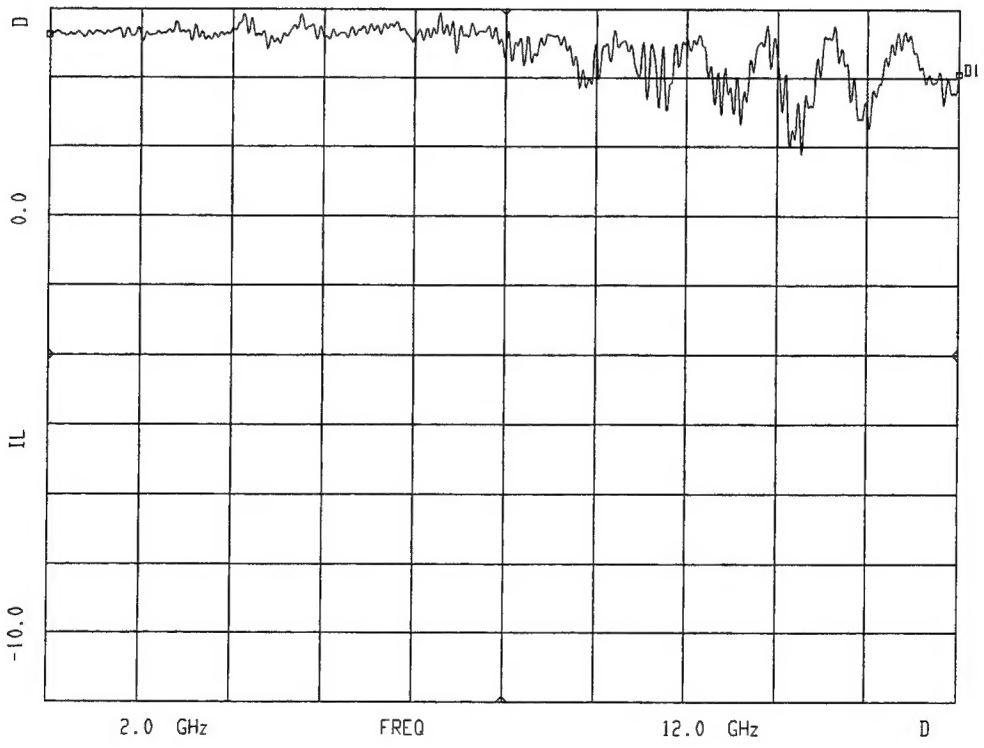


Figure 3 - Insertion loss for a 50Ω line from 2 to 12 GHz. Notice that vertical scale is 1 dB/division. Our connector interface needs to be improved in the X-band region.

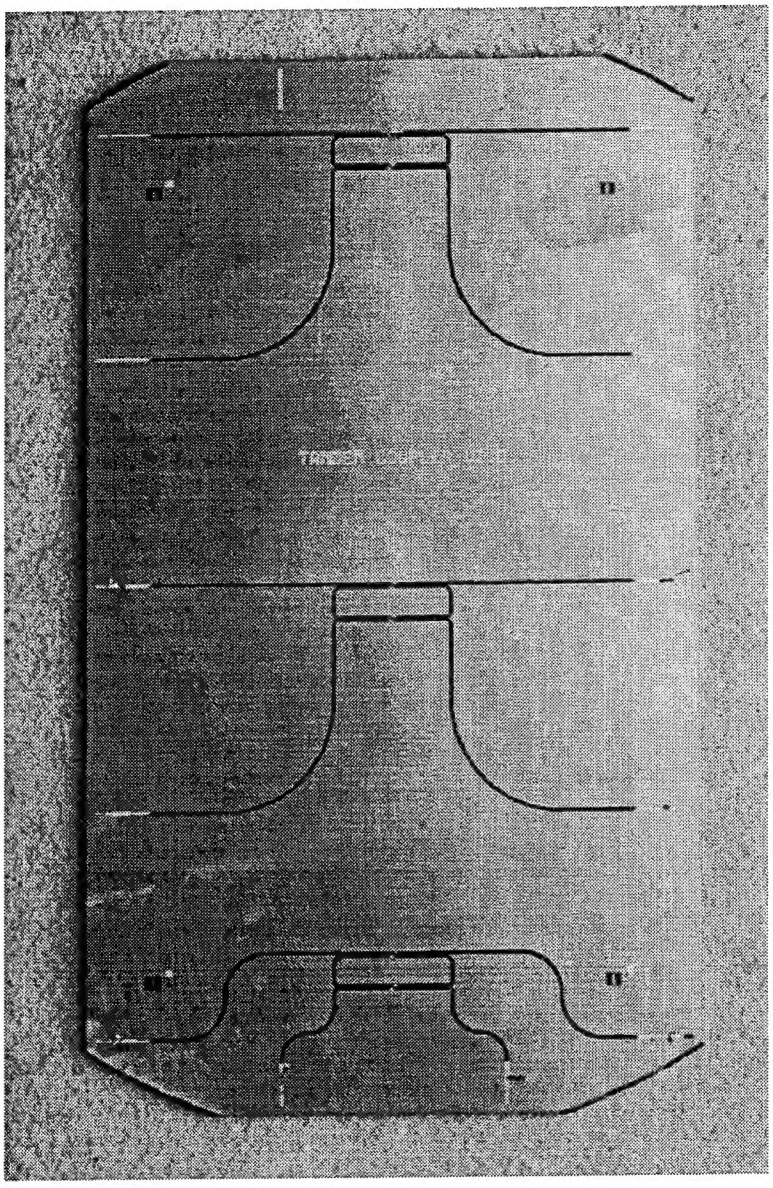


Figure 4 - Photograph of tandem coupler test wafer, showing three couplers.

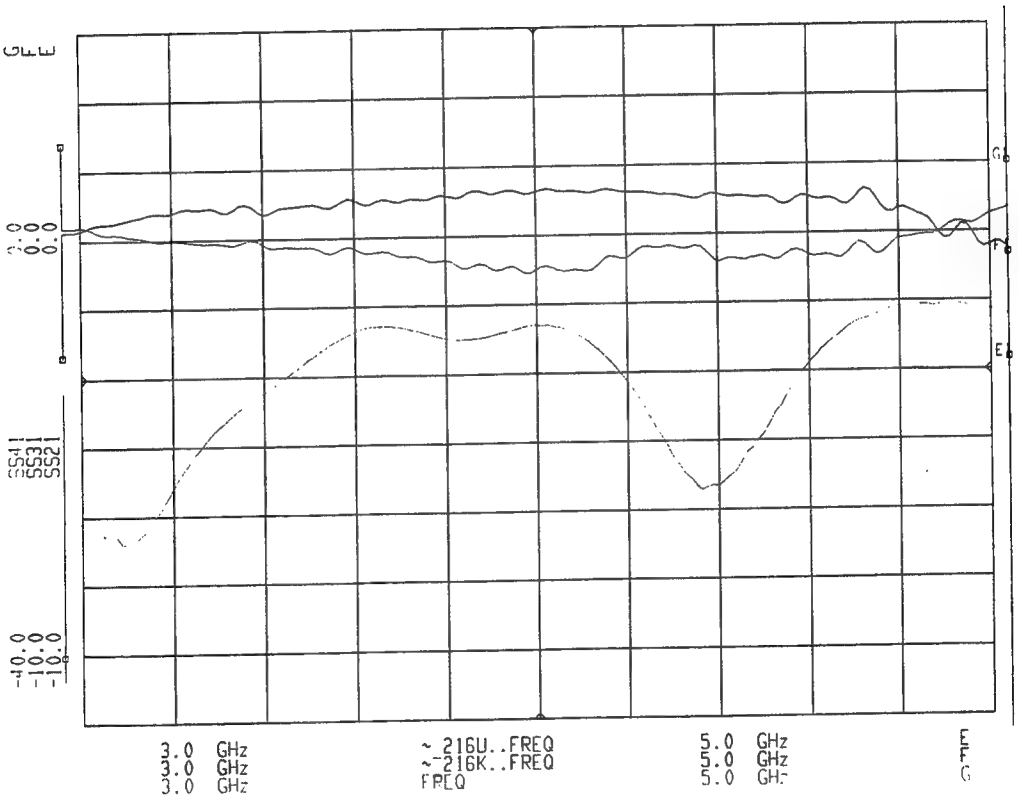


Figure 5 - Test results of the tandem coupler showing 3 dB power split and isolation over a 2 GHz bandwidth.

Overall View of Lump_el

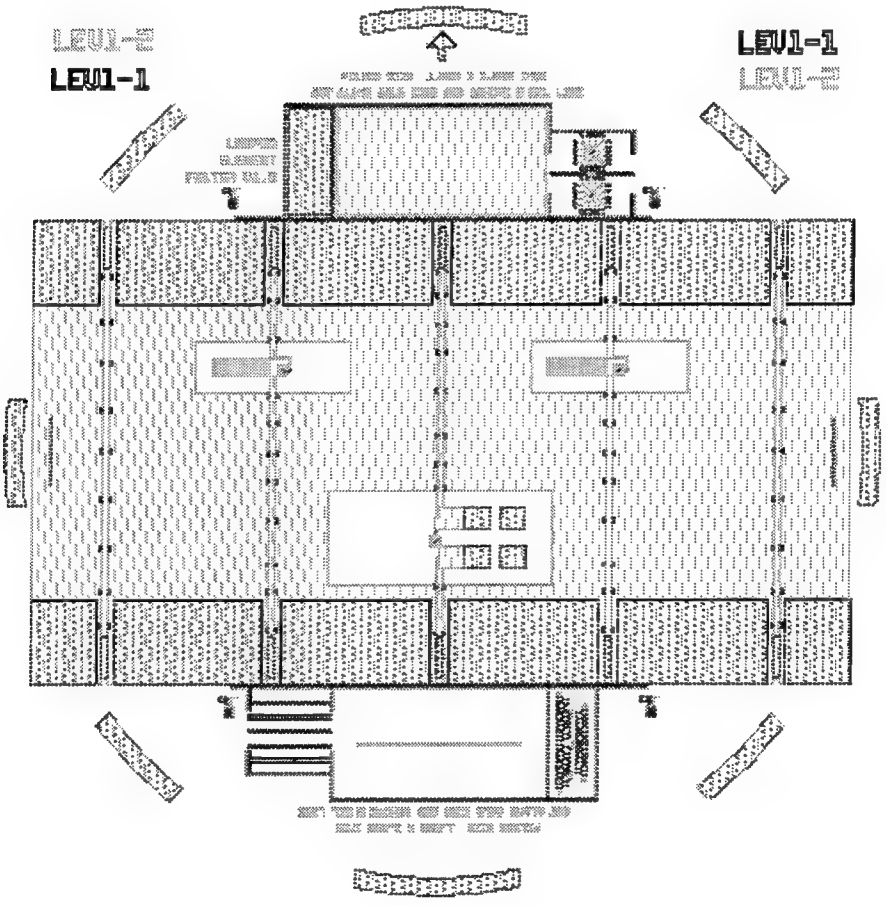


Figure 6 - Mask layout of the lumped element test circuits, showing three series resonators, two (identical) with an interdigitated capacitor and one with gold contact pads for mounting a ceramic chip capacitor.

inductor design: One with an interdigitated capacitor and the other with a ceramic, off-the-shelf capacitor from American Technical Ceramics. Figure 6 shows the mask layout for the test wafer; Figure 7 is a photograph of one of the two wafers made. The measurement results will be reported on in the next quarter.

A size and wafer count comparison was made between a distributed and a lumped-element 40-channel, 3-to-5-GHz EW filterbank. With changes in the architecture the 2-inch diameter wafer count could be cut in half (from 12 to 6). A copy of the study is included in the appendix. It is expected that an initial design cost for the new architecture, which comprises star-multiplexing of groups of channels, will be offset by a much lower wafer count. Future efforts to implement EW channelizers for the entire 2-GHz receiver IF band will use this preliminary study as the basis for more efficient architecture than the one to be used in this program for demonstration purposes.

Delay Lines

A revised substrate mounting technique for delay lines has been tested, yielding improved and more reliable results over a wide band. The technique is based on a preliminary mounting of each substrate making up the stripline structure on its carrier. This allows alignment of both carrier-substrate assemblies. Once alignment is completed, the assembly is heated to a few degrees below the melting point of indium, under spring-loaded pressure. This allows the indium to flow and fill in the voids between substrates and carriers, providing uniform ground return contacts. Since the pressure is maintained after cooling by means of belville washers on screws holding the assembly together, the good contact attained is ensured after the mounting process is finished. This is in contrast with the technique used previously, where the substrates were mounted on their carriers using indium sheets and heat, under an external spring pressure *which was removed after cooling*. Then the substrate-carrier assemblies were aligned with respect to each other and fastened together using the belville washers.

Figure 8 shows the results of a measured response before and after the new technique was applied.

An effort was began to optimize the delay line design to further improve its characteristics and lower the amplitude ripple to below 0.5 dB. Simulations of the

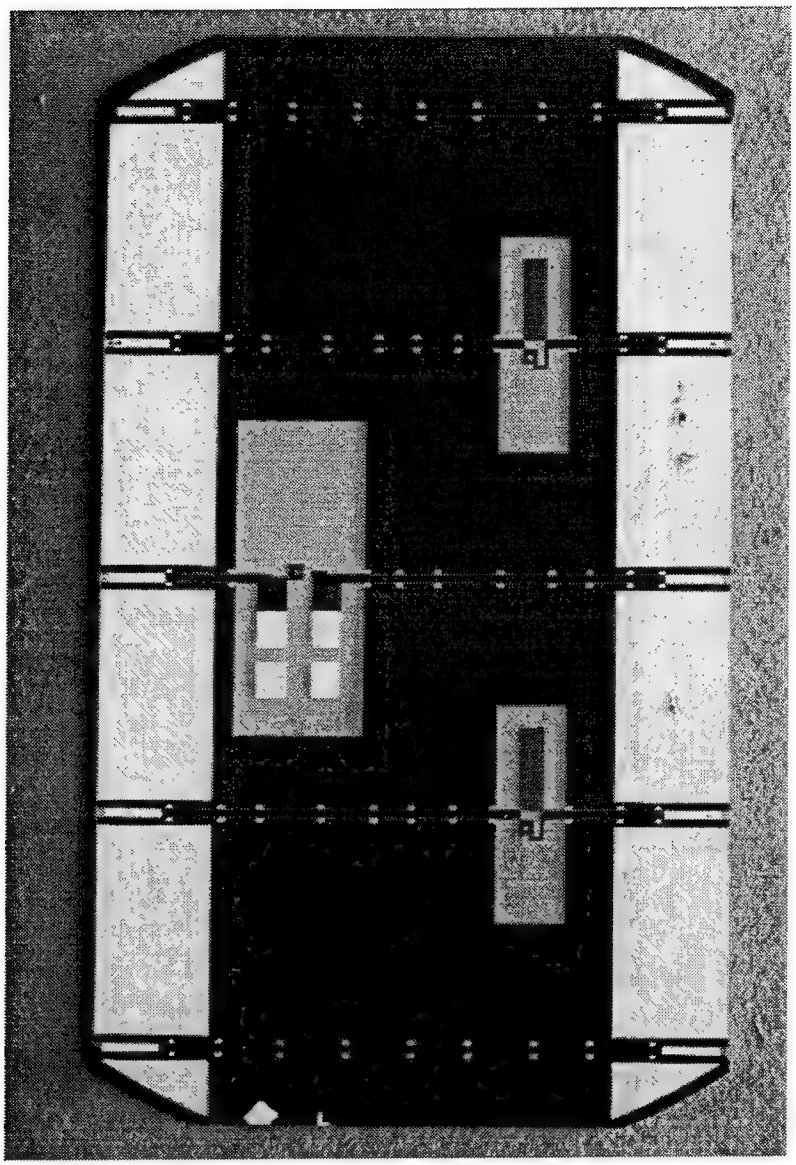


Figure 7 - Photograph of lumped element test wafer.

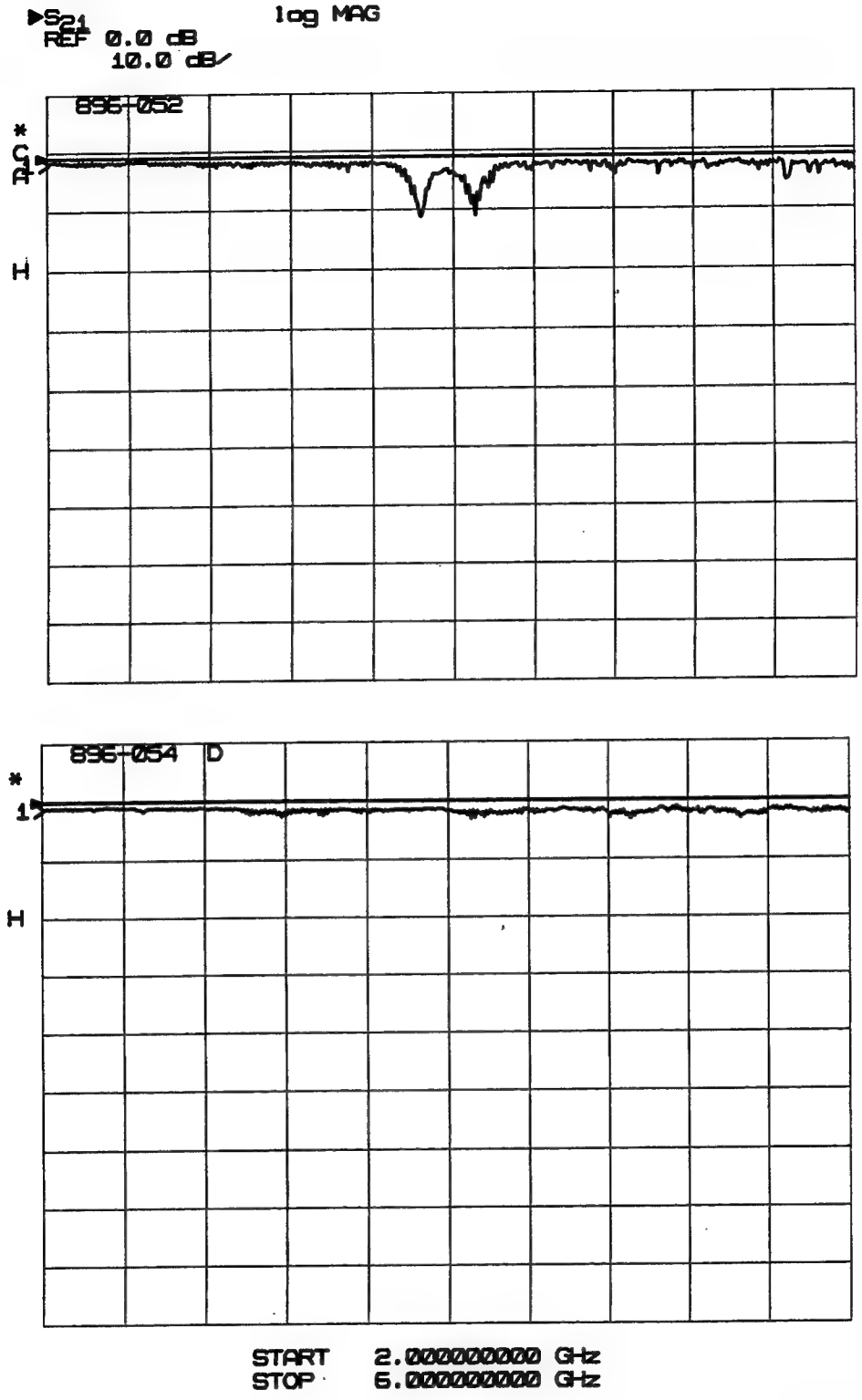


Figure 8 - Insertion loss of delay line mounted with the old technique (top) and the revised assembly procedure (bottom).

launching scheme have begun using the 3D electromagnetic analysis software tool. A new coaxial to coplanar transition design is underway to improve the overall VSWR at the connectors. Results on this analysis will be reported in the next quarter.

TASK 3.1: PVD MULTILAYER FILM FABRICATION

The subtask scheduled for this reporting period required delivery of YBCO films on both sides of two-inch diameter substrates to Task 2.2. A significant result obtained under our Westinghouse/AFOSR program was implemented in this program during the reporting period. The result was that YBCO targets doped with 5 wt. percent Ag produced the lowest R_s(77K, 10 Ghz) films yet made at Westinghouse. The improvement was by approximately a factor of two from the 0.45 to 0.5 mΩ range — achieved with a number of YBCO films on 2" wafers throughout the performance of this program — to a handful of 2" films with the new target in the 0.2 to 0.3 mΩ range. The error for such measurements was reduced early in 1994 to ± 0.05 mΩ.

Films produced with the new target have the microstructural features that we have learned to associate with low-loss YBCO films: no copper-oxide boulders, no a-axis oriented grains, an x-ray rocking curve width < 0.5°, and a clearly-resolved a-b twinning observed by x-ray diffraction which is the most sensitive microstructural test.

The motivation for trying Ag-doped targets was to see whether its incorporation in the film would affect either R_s, the RF power handling of the films, or their noise properties. However, to our surprise, no Ag can be detected in the films. Since there is no question that a measurable improvement was made in R_s, we have tentatively attributed the improvement to changes in the physical properties of the *target* during deposition (better thermal conductivity? electrical conductivity?). Under the AFOSR program, we are attempting to compare the stability of the plasma with that produced at the surface of a standard YBCO target. Meanwhile, we have switched one of the two sputtering chambers used to deposit large-area films to Ag-doped YBCO targets and ordered targets for the second system.

TASK 3.2: MOCVD MULTILAYER FILM FABRICATION

Work at Emcore under this project was completed during the reporting period. The primary objectives of this task were met with demonstrations of R_s-qualified YBCO films grown by MOCVD in a full-scale reactor on both sides of large-area wafers. The number of such wafers was too small to replace sputtered films in all of the devices produced in the program. However, fabrication and successful performance of a filter channel with two filters, two branchline couplers, and integrated thin-film loads demonstrated that the MOCVD films could withstand processing without degrading their desirable microwave properties.

Evaluation of the new Ba precursors developed at Northwestern University will continue there for the first two quarters of 1995 although this task was originally scheduled to be completed by the end of 1994. Evaluation of new precursors in Emcore's full-scale reactor proved to be incompatible with maintaining an optimized deposition system so all of the remaining precursor evaluation will be performed at Northwestern.

The work at Northwestern is focused on a family of liquid, non-fluorinated Ba precursors that sublime at 150°C. The crystal structure of one of the compounds was determined last summer and shown in Report #12. That compound, $BaCF_3CF_3$(CAP-3), used β-diketonate polyglyme ligands to coordinate the Ba ions. A molecule of DMSO solvent was coordinated at each of two sulfur ions. During this quarter, crystals were grown of a related compound which has one additional oxygen. It does not coordinate with any solvent molecules. When it was found that this compound also sublimes at 150° and BaO films were successfully grown at 180°C, a letter was prepared for publication. However, it was later found that some of the precursor decomposes at such temperatures and the communication is being withheld until the pathway to decomposition is understood.

TASK 3.3: RF CHARACTERIZATION OF FILM PROPERTIES

RF surface resistance measurements were made during the quarter on YBCO films on 2-inch wafers at a rate of approximately three per week, approximately half the number of measurements needed in the previous quarter. Measurements were used

either to ensure that sputtered films were qualified for device fabrication or to evaluate films made by MOCVD at Emcore.

The standard measurement of R_s employs a dielectric resonator with a reference YBCO film on a 2" wafer and a film to be measured. Two such resonators are in use with reference films having R_s(77K, 10 GHz) = 0.55 ± 0.04 mW and 0.49 ± 0.04 mW, respectively. A similar accuracy is expected for low-R_s films (<0.5 mW) and better accuracy for higher-R_s films since losses from the reference film become less significant.

TASK 5.0: SWITCHED FILTERBANK

The status of the switch fabrication is given in Table I. The remaining wafer, 1562-4, will be completed using a new etch-back mask (level 58) which has fewer vent lines than originally designed, to avoid undue weakening of the switch die. This followed an analysis performed to confirm the suitability of the vent line length and cross section. Figure 9 shows the layout of a switch with etch-back FETs (EB-FETs). The approximate dimensions and shape of the cavity under each FET is shown in Figure 10. Figure 11 shows the dimensions and location of the existing vent lines and vent membranes (which need to be ruptured to provide venting). The results of the analysis are given in Figure 12, which shows the relative pressure reduction in the membrane as a function of time. That is, the existing membrane and vent line dimensions will allow the pressure on the membranes to be reduced by a factor of ten in a few seconds (1 to 10). This was considered adequate and it was only thought necessary to reduce the number of vent lines in order to ensure the mechanical integrity of the switches.

Table I - Status of Switch Wafer Fabrication

Wafer #	Wafer Type	Status
1562-1	Normal	Completed. Cracked. Usable devices
1562-2	Normal	Completed. Scribed into reticle size pieces
1562-3	Normal	Broken during fabrication
1562-4	Etch Back	In process. New vent mask layer to be used
1562-5	Etch Back	Completed. Some over-etched tubs. Scribed. Some good devices.
1562-6	Etch Back	Completed. Awaiting measurements
1562-7	Etch Back	Completed. Awaiting measurements
1562-8	Etch Back	Completed. Awaiting measurements

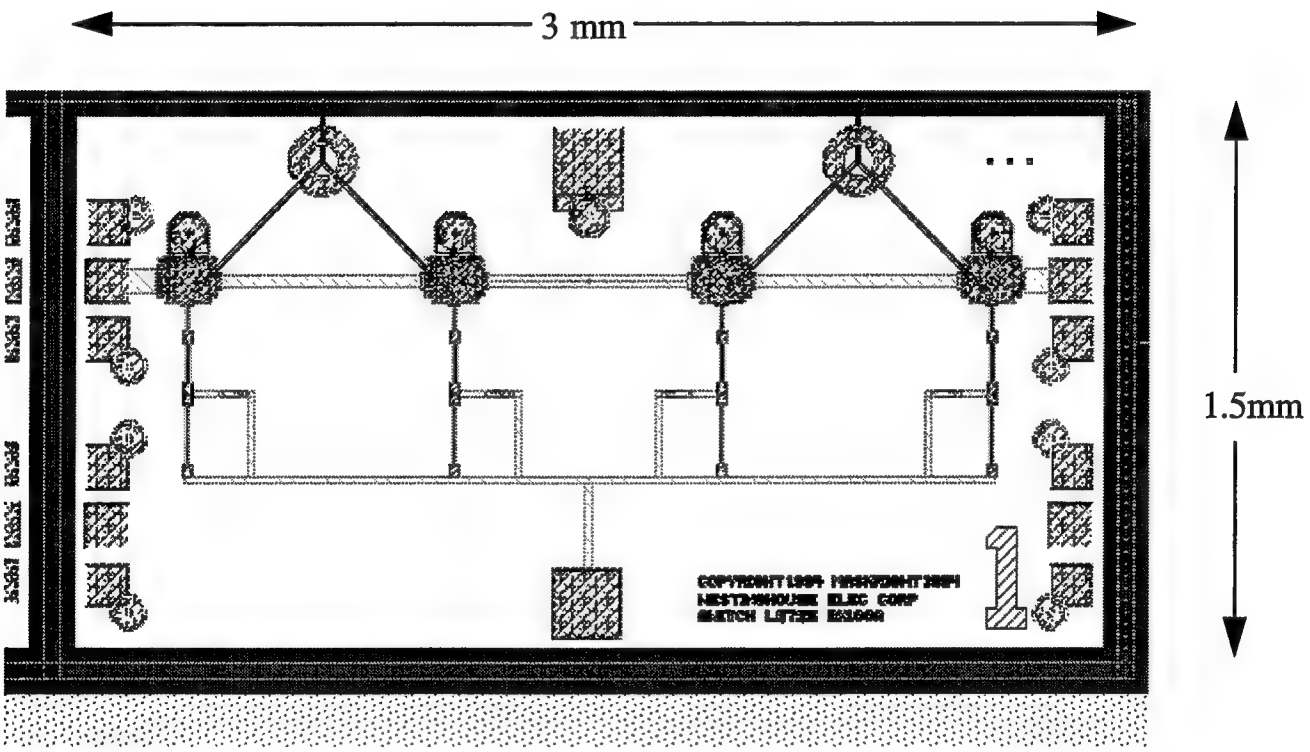


Figure 9 - Layout of one of the Etch-Back FET switch designs.

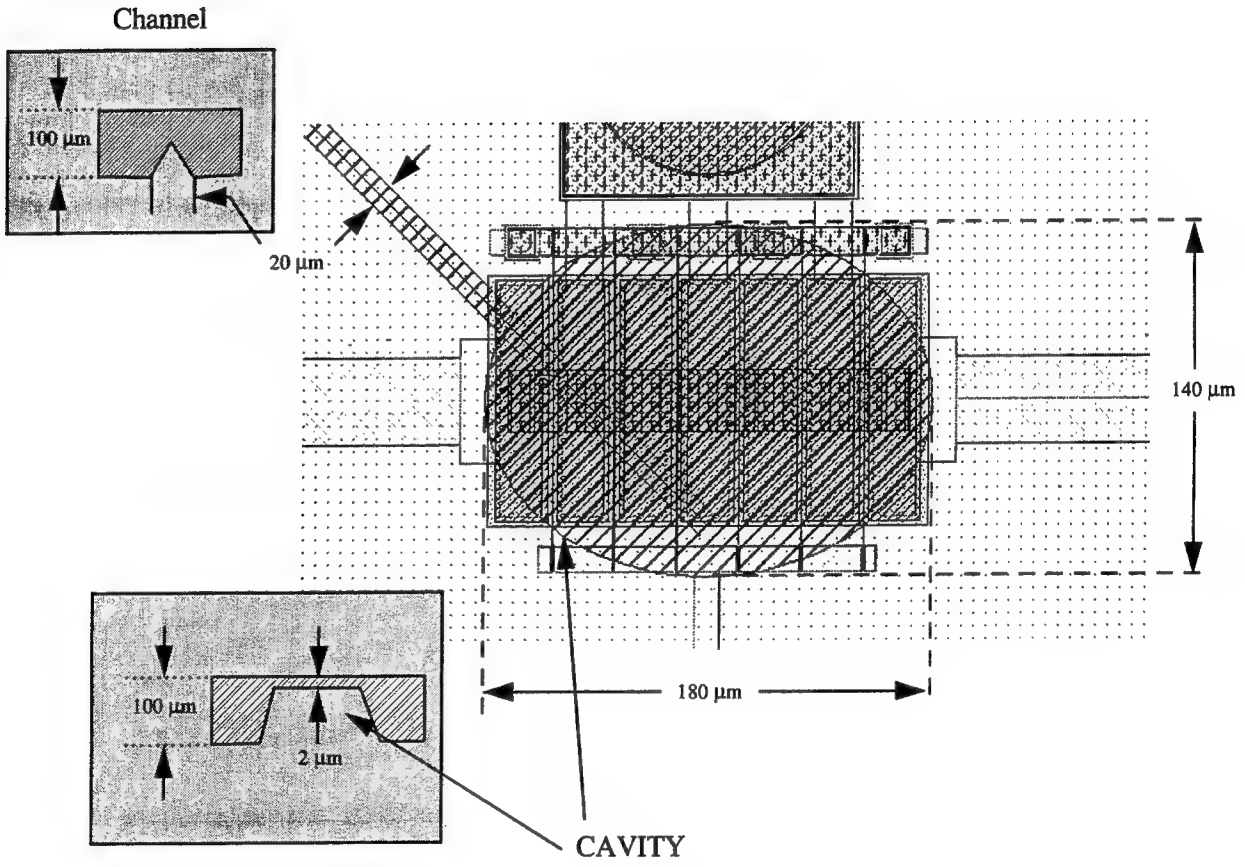


Figure 10 - Etch-Back cavity shape and approximate dimensions.

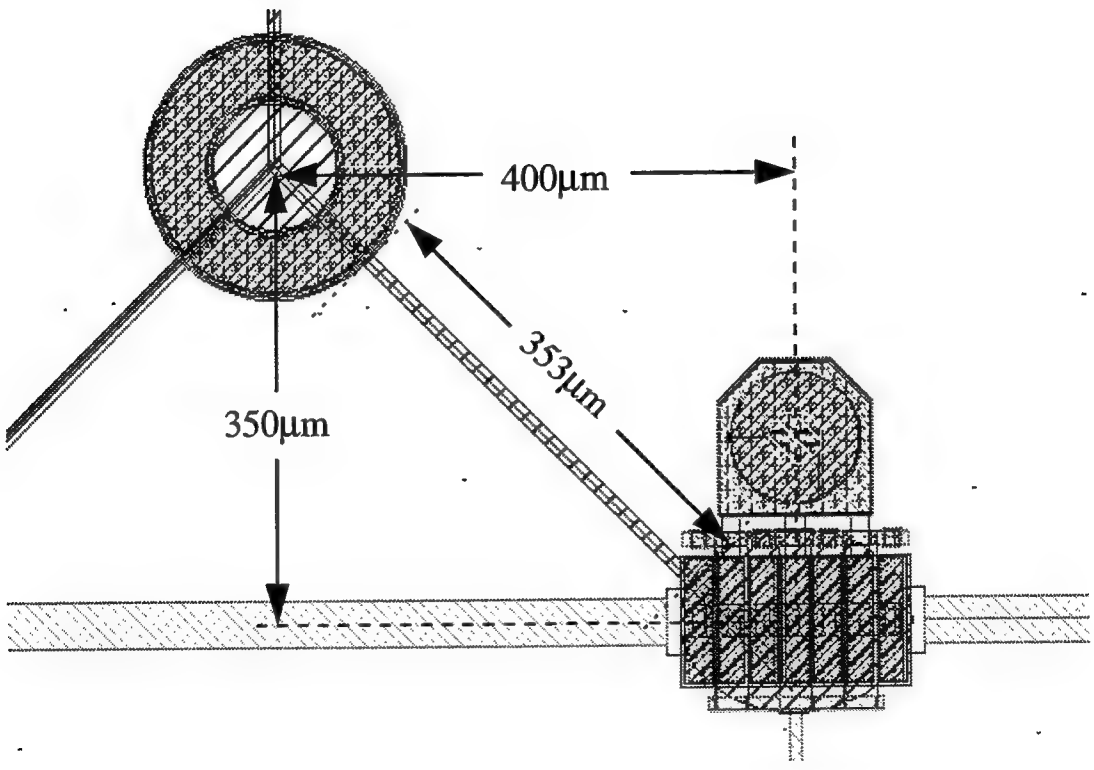
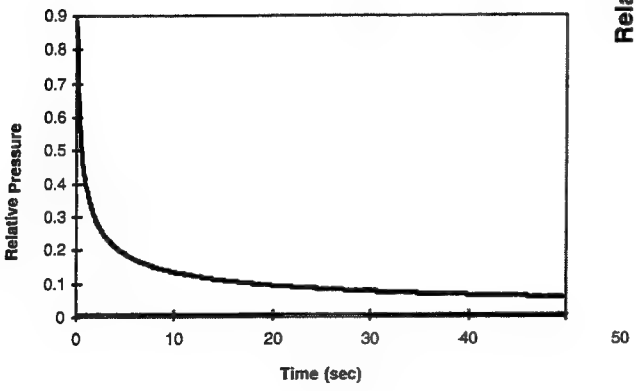


Figure 11 - Dimensions and locations of existing vent lines.

Pressure In Etch Back Cavity

$$\alpha \dot{x} = \frac{P_i}{1 + \frac{Ax}{V_0}} - P_0$$

P_i=14 psi, A=170 μ^2, V_o=140x180X100 μ^3,
α=14/40000 psi sec/μ, P_o=0



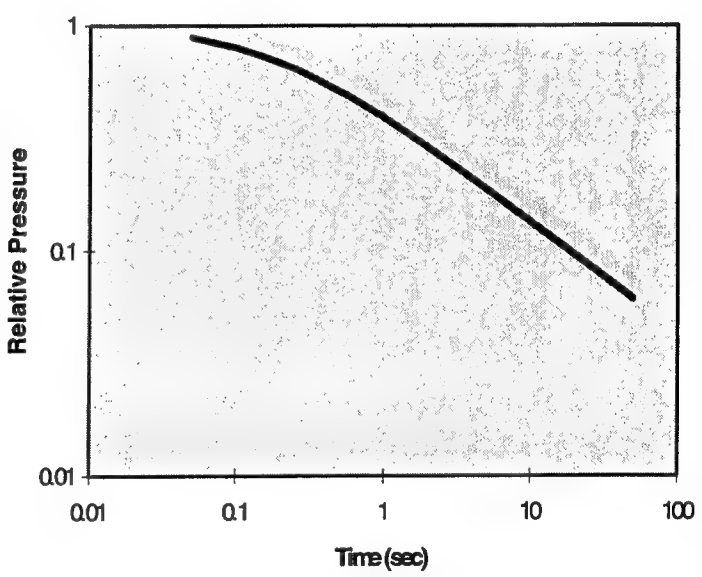


Figure 12 - Results of Etch-Back cavity venting analysis.

Measurements of the switch C_{off} capacitance for the wafers with etch-stop layers, before and after membrane etching yielded a reduction of nearly 50%, as designed. Figure 13 shows these measurements.

Some of the EB-FETs from the finished wafers have been measured as well, showing excellent characteristics at room temperature. Figure 14 shows the isolation and insertion loss of a sample switch device. At 10 GHz, the isolation is greater than 70 dB and the insertion loss about 0.45 dB. The results to date represent an advancement in the GaAs switch state of the art.

Sample switches with EB-FETs will be tested at cryogenic temperatures in the next quarter.

Preparations for measurements of the switches in filter packages are also being made. The first step will be to measure them between two 50-Ω superconducting microstrip lines. A mask layout for 2-inch diameter, 20 mil thick LAO wafers has been designed with these lines, as shown in Figure 15. Fabrication and testing, at first with normal FET switches, will be carried out in the next quarter.

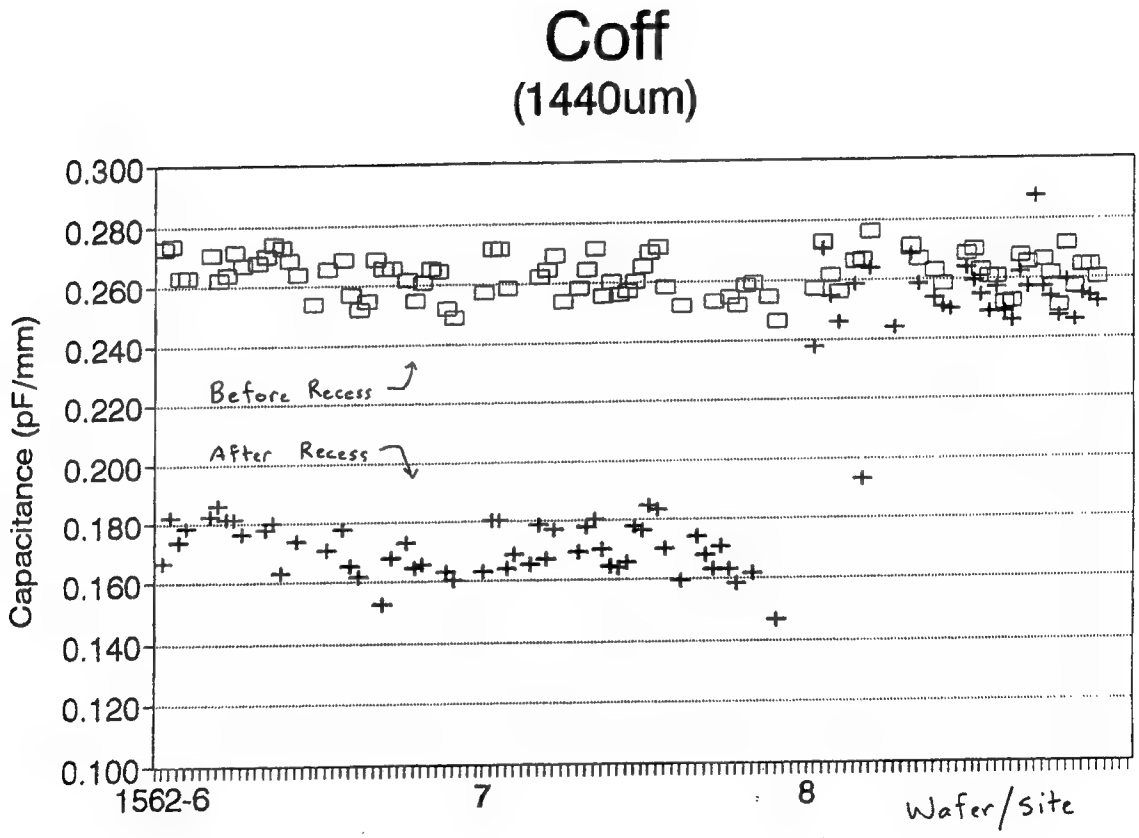


Figure 13 C_{off} measurement comparison between normal and Etch-Back FETs.

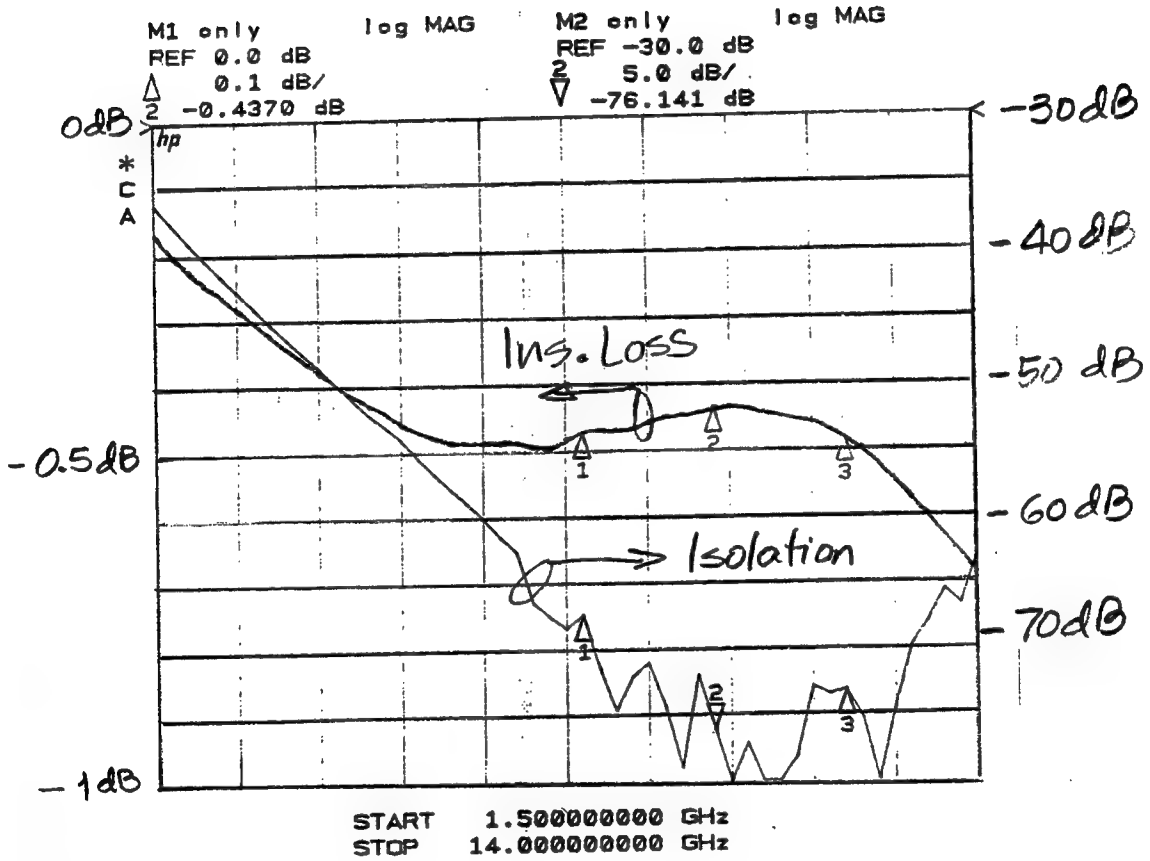
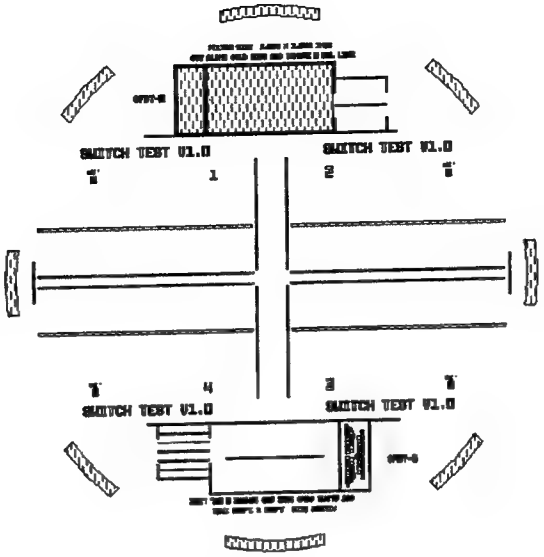


Figure 14 - Insertion loss and isolation measurements at room temperature for one of the Etch-Back FET switches.



Upper Right Quadrant of 50 Ohm
Switched filter Bank Straight Through
All Dimensions in µm

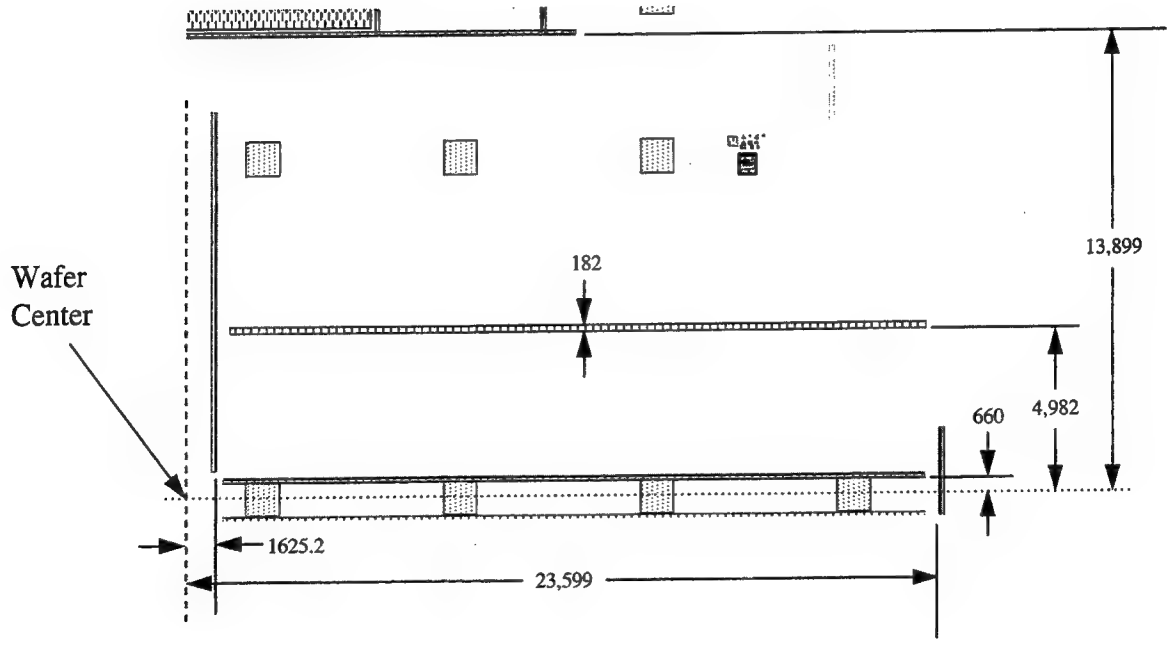


Figure 15 - Mask layout for the testing of switches between HTS temperature lines.

Appendix

FILTER BANK CONSTRUCTION DISCUSSION

This is a discussion of assembly trade-offs in the design of a cryogenic filter bank. The filter bank design has one 3-5 GHz wideband input, which is filtered into forty independent 50 MHz channels. All forty outputs are available simultaneously.

SINGLE FILTER DESIGN TECHNIQUES

Each filter in the forty channel bank will have a cosine-cubed, 7 pole response with a 3 dB bandwidth of 50 MHz. Center frequencies will span the range from 3 to 5 GHz. The design can be implemented with lumped techniques or distributed. A distributed filter design uses coupled transmission line resonators to implement the filter. The lumped design uses printed inductors and capacitors. At lower frequencies, the lumped filter design tends to require less space for its implementation. The less space the design requires, the less LAO is required, yielding cost reductions. There are some other distributed design techniques which use more exotic implementations of the resonators (eighth wave resonators, resonant lumped copper pads, and others), which can offer size reductions for distributed filter implementations relative to the lumped versions. However, these techniques are still under development, and the tools and techniques are still limited to estimates and some trial and error. This would be quite an expensive process on LAO with 40 filters to develop.

For the design considered here, an estimate can be made of the size of the lumped and distributed filter implementations on LAO. These estimates are based on completed designs, and use appropriate scaling to relate them to the requirements here.

SINGLE FILTER LAYOUT AREA

Frequency (GHz)	Lumped Design Area (Inches^2)	Distributed Design Area (Inches^2)
3	.4	.8
4	.33	.6
5	.25	.48

As can be seen in the above table, lumped designs will offer a 2:1 space improvement compared to end coupled half wave resonator distributed filter designs.

FILTER BANK ARCHITECTURES

There are several different topologies suitable for the 40 channel filter bank. Some of these options are shown schematically in Figures 1-4.

Figure 1 shows the schematic for a quadrature arrangement of the filters. This topolgy allows each filter to be properly terminated in 50 ohms via isolation of the quadrature combining. Thus, the measured response from a single channel in the filter bank will be identical to that of a single filter in a 50 ohm system. The loss of this design will be no lower than 3 dB due to the input splitter, which splits the even and odd channels. This eliminates the need to design for effects of filter interactions. While it presents the most simplest design, suitable for use with lumped or distributed filters, it also requires double the amount of filters (80), as each quadrature hybrid must be loaded with an identical filter. The performance of this system will also degrade if the response of the two identical filters do not exactly match each other in phase and amplitude.

Figure 2 shows a ferrite implementation of the filter bank. This configuration also offers the filter-to-filter interaction isolation as the Figure 1 topology. It requires the use of a circulator for each filter however. The ideal loss of this topology could be 0 dB, as no splitting loss is required. While circulators are being fabricated for cryogenic use, their size will be quite large at the 3-5 GHz frequency band. The size of these components will be the major limitation in the use of this topology.

Figure 3 shows a topology which could be implemented using lumped filter construction. This design would be quite difficult however, as all filters will be interacting with each other, an effect which must be accounted for in the design. The ideal loss of this topology is 0 dB. One important consideration is the distance of the filters relative to the common input feed. Any excess distances will transform the out of band filter impedances, making the filter interaction design problem even more difficult. Because of this, the topology is most easily implemented in the form of a star, as shown in Figure 5, to minimize the distances between inputs. As the number of filters increase, this topology will become increasingly difficult to implement however, as each filter will become close to its neighbors.

Figure 4 shows a topology similar to the previous star topology, except the 3 dB splitter is brought back to separate even and odd channels. This limits the ideal minimum loss to 3 dB. The splitter puts a passband of space between filters, which translates to lessened interaction effects easing the design. It also halves the number of filters in the star assembly (although the total is still the same), easing assembly considerations. The center frequency filters in each half-star assembly will be relatively unaffected by their neighbors. This is because the number of filters above the center frequency contribute an approximately equal and opposite reactance as the number of filters below the center frequency filters. The opposite is true on the first and last filters, however. This effect is shown for a paper designed 4 filter star arrangement shown in Figure 6. With proper design considerations, it is felt these interactions could be accounted for.

The required amount of LAO needed for fabricating a 40 channel filter bank can be estimated based on the number of filters and quadrature hybrids needed for each configuration. This is given below in terms of numbers of 2 inch wafers needed, assuming each wafer of LAO has 2.54 inches^2 of available area.

ARCHITECTURE (Figure#)	# LAO 2" WAFERS	COMMENTS
Quadrature(1)-Lumped	20	3dB loss, 80 filters
Quadrature(1)-Distributed	12	3dB loss, 80 filters
Circulators(2)-Lumped	19	0dB loss, 40 filters, Circulator development
Circulators(2)-Distributed	15	0dB loss, 40 filters, Circulator development
Full Chain Lumped(3) (Star)	6	0dB loss, 40 filters, Difficult assembly
Half Chain Lumped(4) (Half-star)	6	3dB loss, 40 filters

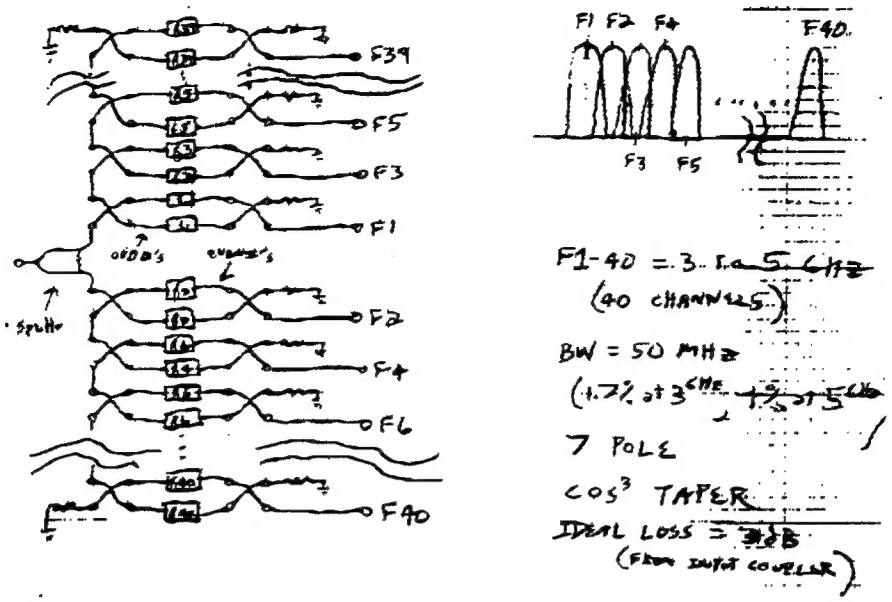


FIGURE 1

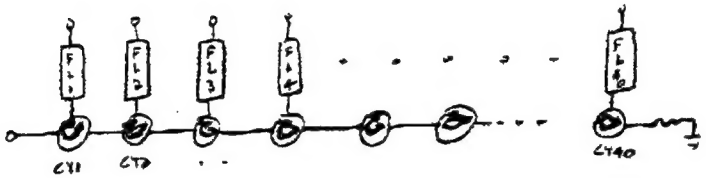
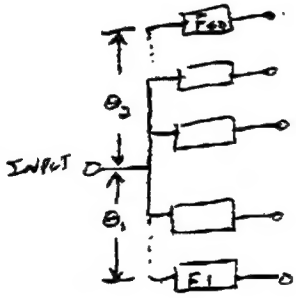
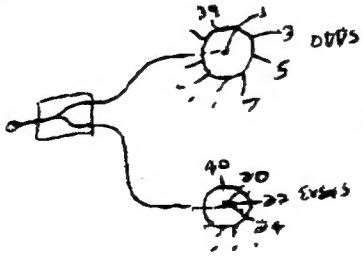


FIGURE 2



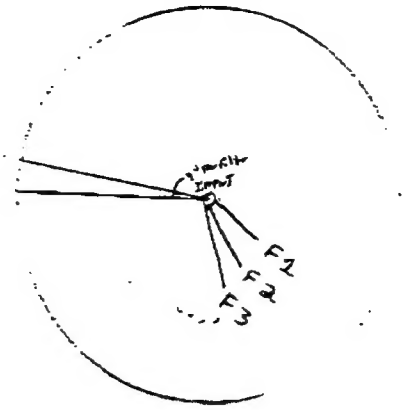
THIS OFFERS A REDUCTION IN THE NUMBER OF FILTERS BY A FACTOR OF 2.

FIGURE 3



THIS OFFERS REDUCED RISK FROM PREVIOUS OPTION, AS ALL FILTERS ARE MORE DISTANT FROM EACH OTHER ON THE IMPEDANCE PLANE

Figure 4



THIS IS NOT INOUCH Room FOR A PLANAR IMPLEMENTATION,
BUT IT COULD BE implemented by placing boards on edge :

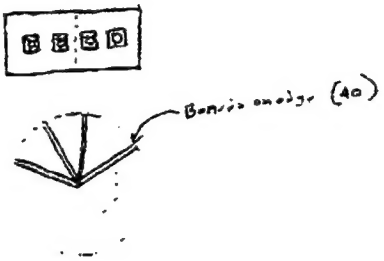


Figure 5

SERIES CIRCUIT INPUT

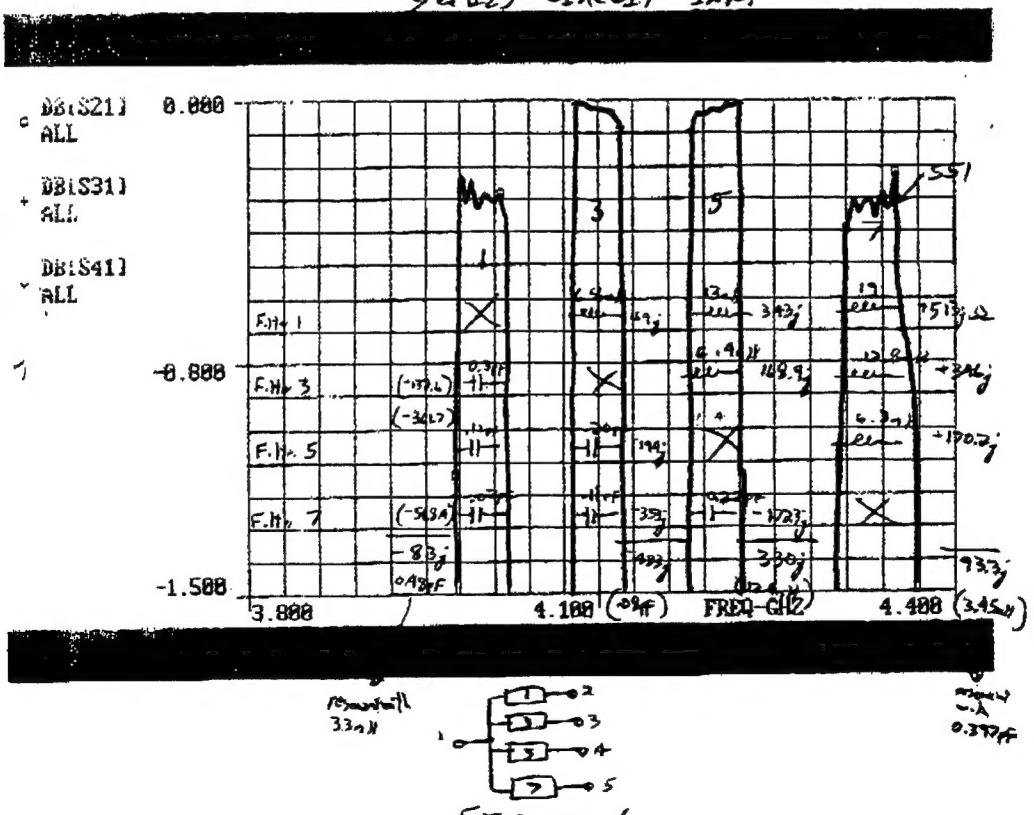


FIG. 6